UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/085,222	02/28/2002	David B. Kramer	9-22	6946

7590 08/21/2006

Ryan, Mason & Lewis, LLP
90 Forest Avenue
Locust Valley, NY 11560

EXAMINER	
TSEGAYE, SABA	

ART UNIT	PAPER NUMBER
2616	

DATE MAILED: 08/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/085,222	KRAMER ET AL.	
	Examiner	Art Unit	
	Saba Tsegaye	2616	

-- The MAILING DATE of this communicati n appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This office Action is in response to the amendment filed 06/02/06. Claims 1-21 are pending. Currently no claims are in condition for allowance.

Claim Rejections - 35 USC § 103

2. Claims 1, 2, 4-18, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fan et al. (US 6,389,019) in view of Willard (US 6,374,405 B1).

Regarding claim 1, 2, 10, and 20, Fan discloses, in Figs. 2 and 3, a processor comprising:

scheduling circuitry (6) for scheduling data blocks for transmission from a plurality of transmission elements (scheduling stream queues serving cells with different QoS within an ATM switch), the scheduling circuitry being configurable for utilization of at least one time slot table (5AB, to handle a large range of bit rates, a plurality of time wheels are employed with different time granularities) in scheduling the data blocks for transmission (scheduler unit selects a stream queue to be services, based on the queue information (abstract; column 6, lines 10-16)); and

an interval computation element (a rate computation unit 8) associated with the scheduling circuitry (6) and operative to determine an interval for transmission of one or more data blocks associated with corresponding locations in the time slot table (the rate computation unit computes the rate for each stream queue that are assigned dynamically to the time wheels based on computed rate values), a particular location in the time slot table being assigned to one or more of the transmission elements as a function of both a current time and the transmission

interval (column 8, line 61-column 9, line6; column 9, lines 10-21), the transmission interval being adjustable under control of the interval computation element (column 3, lines 45-50) so as to facilitate the maintenance of a desired service level for one or more of the transmission elements (column 3, lines 30-64; column 18, line 38-column 19, line 5).

Fan does not expressly disclose that the interval computation element comprises a software-implemented element external to the hardware-implemented scheduler. However those skilled in the art will know that various functions may be performed by software and/or hardware.

Willard teaches a scheduler implemented in software, firmware, hardware or a combination thereof. The scheduler may consist of a delivery time calculator, a start time calculator and a controller (column 6, line 50-column 7, line 12).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the teachings from Willard of using the combination of software-implemented element and hardware-implemented scheduler to the time-base scheduler discloses by Fan. One of ordinary skill in the art would have been motivated to do this because using the combination of software and hardware system provides a flexible and scalable architecture, improves performance and provides extended lifespan of the device.

Regarding claim 4, Fan discloses the processor wherein the interval computation element is operative to determine periodically if the transmission interval requires adjustment in order to maintain the desired service level for one or more of the transmission elements (column 3, lines 45-66).

Regarding claim 5, Fan discloses the processor wherein the interval computation element makes a determination as to whether the transmission interval requires adjustment, after transmission of a specified number of the data blocks (column 16, lines 42-47).

Regarding claim 6, Fan discloses the processor wherein the interval computation element makes a determination as to whether the transmission interval requires adjustment, after transmission of each of the data blocks (column 5, lines 60-67).

Regarding claim 7, Fan discloses the processor wherein the transmission interval specifies a rate at which data blocks associated with corresponding locations in the time slot table are transmitted (column 3, lines 6-8).

Regarding claim 8, Fan discloses the processor wherein the interval computation element is operative to select the transmission interval from at least a first transmission interval associated with a first scheduling algorithm and a second transmission interval associated with a second scheduling algorithm (column 9, line 54-column 10 line 21).

Regarding claim 9, Fan discloses the processor wherein a given requesting transmission element is assigned to a location in the time slot table in accordance with the following equation:

Assigned Time Slot=Current Time +Interval,

Where current time denotes a time corresponding to a current transmission time slot and Interval denotes the transmission interval (column 9, lines 1-2; column 7, lines 2-21).

Regarding claim 11, Fan discloses the processor further comprising traffic shaping circuitry (8) coupled to the scheduling circuitry (6), the traffic shaping circuitry comprising the interval computation element (column 6, lines 6-10).

Regarding claim 12, Fan discloses (Fig. 1) the processor further comprising transmit queue circuitry (2) coupled to the scheduling circuitry (3), wherein the transmission elements comprise one or more queues (1) associated with the transmit queue circuitry, the transmit queue circuitry supplying time slot requests from the transmission elements to the scheduling circuitry in accordance with the a traffic shaping requirement established by the traffic shaping circuitry (column 5, lines 5-45).

Regarding claim 13, Fan discloses the processor wherein the time slot table is stored at least in par in an internal memory of the processor (see fig. 2, 5A).

Regarding claim 14, Fan discloses the processor (6) wherein the time slot table (Time Wheel) is stored at least in part in an external memory (5A) coupled to the processor.

Regarding claim 15, Fan discloses the processor wherein one or more of the data blocks (data stream) (comprise data packets (data cells) (column 5, lines 45-49).

Regarding claim 16, Fan discloses the processor wherein the scheduling circuitry provides dynamic maintenance of the time slot table such that identifiers of requesting

transmission elements are entered into the table locations on a demand bases (the time wheel stricture is augmented with a plurality of priority levels (column 3, lines 1-9; column 18, lines 24-31).

Regarding claim 17, Fan discloses wherein the identifiers of the transmission elements comprise a structure having one or more bits for allowing a given one of the transmission element identifiers to be linked to another r of the transmission element identifiers (column 11, lines 43-54).

Regarding claim 18, Fan discloses the processor wherein the processor configured to provide an interface for data block transfer between a network and a switch fabric (column 2, lines 41-43; column 6, lines 36-40).

Regarding claim 21, Fan in view of Willard discloses all the claim limitation as stated above except for a machine-readable storage medium for use in conjunction with a processor.

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use software-base machines, the benefit using machine-readable device is that programs cha be changed and upgraded and new futures are added easily than hardware changes.

3. Claims 1, 4, 14, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boland et al. (US 5,889,763) in view of Willard (US 6,374,405 B1).

Regarding claims 1, 4 and 20, Boland discloses, in Fig. 1, a processor comprising:

scheduling circuitry (12) for scheduling data blocks for transmission from a plurality of transmission elements (column 3, lines 17-21), the scheduling circuitry being configurable for utilization of at least one time slot table (100, 200) in scheduling the data blocks for transmission (column 5, lines 15-30); and

an interval computation element (scheduler 12 comprises a unit that calculates..) associated with the scheduling circuitry (12) and operative to determine an interval for transmission of one or more data blocks associated with corresponding locations in the time slot table (column 3, lines 21-27), the transmission interval being adjustable under control of the interval computation element (column 5, lines 25-30) so as to facilitate the maintenance of a desired service level for one or more of the transmission elements (column 5, lines 15-30; column 6, lines 9-25).

Boland does not expressly disclose that the interval computation element comprises a software-implemented element external to the hardware-implemented scheduler. However those skilled in the art will know that various functions may be performed by software and/or hardware.

Willard teaches a scheduler implemented in software, firmware, hardware or a combination thereof. The scheduler may consist of a delivery time calculator, a start time calculator and a controller (column 6, line 50-column 7, line 12).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the teachings from Willard of using the combination of software-implemented element and hardware-implemented scheduler to the time-base scheduler discloses by Boland.

One of ordinary skill in the art would have been motivated to do this because using the combination of software and hardware system provides a flexible and scalable architecture, improves performance and provides extended lifespan of the device.

Regarding claim 14, Bolond discloses the processor (12) wherein the time slot table is stored at least in part in an external memory coupled to the processor (100, 200, see fig. 1).

Regarding claim 19, Bolond discloses the processor wherein the processor is configured as an integrated circuit (column 1, lines 4-7).

4. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fan in view of Willard as applied to claim 1 above, and further in view of Pool et al. (US 5,455,948).

Fan in view of Willard discloses all the claim limitation as stated above; except for the interval computation element comprises a scrip processor.

Pool teaches a processor wherein priority computation element comprises of a script processor (fig. 3, the processor contains a script processor and scheduler for job queuing and scheduling and communicating with hosts, column 7, lines 6-18). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement a script processor, such as suggested by Pool, in the rate computation unit of Fan in view of Willard in order to compute rate under software control. The benefit of software is that programs can be changed and upgraded and new futures added easily than hardware changes.

5. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fan in view of Willard as applied to claim 1 above, and further in view of Boland et al. (US 5,889,763).

Fan in view of Willard discloses all the claim limitations as stated above except for the processor is configured as and integrated circuit.

Boland teaches a transfer rate controller that is configured as an integrated circuit (column 1, lines 4-7). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement a processor in the form of an integrated circuit, such as suggested by Boland, in the system of Fan in view of Willard in order to minimize cost and space.

Response to Arguments

6. Applicant's arguments with respect to claims 1-21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saba Tsegaye whose telephone number is (571) 272-3091. The examiner can normally be reached on Monday-Friday (7:30-5:00), First Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Doris To can be reached on (571) 272-7629. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ST
August 8, 2006

DORIS H. TO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600